AMENDMENTS TO THE SPECIFICATION

Amend paragraphs [0004] and [0005]:

[0004] Because of high sheet resistance, these ESD diodes must be made large in order to discharge the ESD currents. However, in a CMOS technology, this also leads to an increase in the capacitance per unit area which is acceptable for CMOS technologies below 1 Ghz application frequencies but not for application speeds above this frequency range. Large ESD structures are also unacceptable for high speed RF applications due to the high capacitance load placed on the RF circuit. U.S. Patent ~~4,734,271~~ 4,736,271 to Mack et al., "Protection Device Utilizing One or More Subsurface Diodes and Associated Method of Manufacture," teaches ESD diodes vertically formed in the substrate. As shown in Figs. 4A and 4B of this patent, the pn junctions 46 and 56, respectively, are buried beneath the surface of the substrate. Such structures are used to reduce total surface area consumed by the ESD device. U.S. Patent 5,825,067 to Takeuchi et al., entitled "Dielectrically Isolated IC Merged with Surge Protection Circuit and Method For Manufacturing the Same" teaches forming a simple ESD diode in a well region completely isolated from the substrate. Such an arrangement improves latchup immunity because the device is physically completely isolated from the substrate, at the expense of extra processing steps and complexity associated with providing such complete isolation.

[0005] As ~~integrrated~~ integrated circuit (IC) switching speeds improve, it is important to provide ESD diodes with high Quality factors, known as "Q" . The Q factor in an ESD diode is a function of the capacitance and the diode series resistance. For ESD robustness and a high Q factor, it is important to provide an ESD element which has a ~~minium~~ minimum of diode resistance and inductance.